Space Vector Modulation Based on Classification Method in Three-Phase Multi-level Voltage Source Inverters

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Abstract **- Space Vector Modulation (SVM) is commonly used in digital implementations of three phase PWM modulators. This paper proposes a general approach to determining sectors and durations associated with SVM in multi-level inverters. The algorithm is exact, fast, and applicable to any number of levels. It is based on a vector classification technique, which allows determination of the switching sequences and the calculation the switching instants in m-level inverters. The proposed technique reduces software complexity, decreases the computation time, and increases the accuracy of the positioning of the switching instants, when compared with the conventional implementation of the SVM in multi-level converters. Results are given for a 3-level inverter.**

I. Introduction

With the introduction of multi-level voltage-source converters [1], various modulation techniques have been developed for pulse width modulation (PWM). Among these, the space vector PWM provides a number of alternative choices of switching vectors whose time average over one switching period equals a sampled reference voltage vector. In addition, patterns are such as to make the dc side capacitor voltages balanced, which is a very important consideration for proper operation of multi-level converters [2]. This capability, along with its inherent real time PWM ability make the space vector modulation technique an appropriate PWM technique for digital implementation in multi-level structures [3,4].

It has recently been demonstrated that the space vector modulation can be implemented on traditional two-level converters using a classification technique. The classification algorithm requires less computational effort, and as a result, less computational time, when compared with the conventional SVM methods. The technique does not compromise accuracy, and guarantees exact positioning of the switching instants [5,6].

Software and hardware complexity of the SVM increases significantly with the number of converter levels. Also, more non-linear function approximation and therefore less accurate positioning of switching instants occur as the number of converter levels increase [7,8].

The classification algorithm can be of major help in implementing fast and exact positioning of switching state vectors in multi-level converters. This paper introduces a generalized classification algorithm for a general *m*-level voltage-source converter.

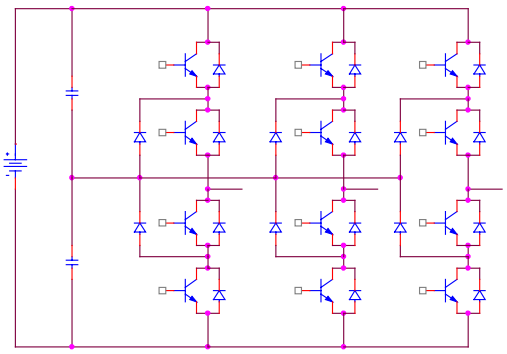

Fig. 1. Schematic diagram of a 3-level voltage source inverter.

The proposed technique employs a classifier network to distinguish between 6 $(m\text{-}1)^2$ separate decision areas, in which the tip of the reference voltage vector lies. Also non-linear functions and time-consuming calculations are avoided. The on-durations of the switching state vectors are obtained from mathematical operators by simple multiplications and additions. The paper presents a theoretical basis for the classification SVM technique. Results are confirmed by implementation on a simulator for a 3-level inverter.

II. The Classification Algorithm

It is shown in [5,6], that the SVM can be implemented by a simple and accurate algorithm based on classification techniques such as are found in neural network theory [10]. The adjacent vectors required to synthesize the reference vector are obtained by computing vector products, and choosing combination that yields the largest value. The time duration is obtained as a result of the calculations.

This paper generalizes these results.

III. Proposed SVM Implementation for a 3-Level DCMI

A. Three-Level Inverter Topology and Switching States

Fig. 1 shows a schematic diagram of a 3-level voltage source inverter. The 3-level inverter has 27 $(=3^3)$ permitted switching states [9]. The application of the Park Transformation [9] to the 27 permitted switching states of the inverter results in 18 non-zero active voltage space vectors ($V_k, k = 1, 2,\ldots,18$) forming a two-layer hexagon centered at the origin of the $\alpha\beta$ plane and a

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zero voltage vector located at the origin of the plane, as depicted in Fig. 2.

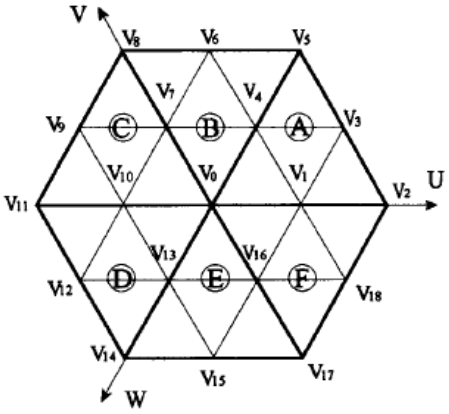


Fig. 2. Switching states of a 3-level inverter.

B. Voltage Vectors and Their Durations

To minimize the harmonic components of the output voltage and current in the SVM technique, the output voltage vector is synthesized by the three nearest active switching vectors adjacent to it. The on-duration of each switching vector is given by the SVM strategy [3]. For example in Fig. 3, and in triangle #3 we have,

$$\underline{V}_{ref}T = \underline{V}_1 t_1 + \underline{V}_3 t_3 + \underline{V}_4 t_4 \quad , \quad \underline{V}_{ref} = V(\cos\theta + i\sin\theta)$$
$$t_1 + t_3 + t_4 = T \qquad\qquad V = \left|\underline{V}_{ref}\right| \tag{1-a}$$

$$\underline{V}_1 = E/2 \quad , \underline{V}_3 = E\sqrt{3}/2 \cdot e^{i\frac{\pi}{6}} \quad , \underline{V}_4 = E/2 \cdot e^{i\frac{\pi}{3}} \tag{1-b}$$

$$\begin{bmatrix} t_1 \\ t_3 \\ t_4 \end{bmatrix} = \begin{bmatrix} T & 0 & -\frac{4}{\sqrt{3}}V\frac{T}{E} \\ -T & 2V\frac{T}{E} & \frac{2}{\sqrt{3}}V\frac{T}{E} \\ T & -2V\frac{T}{E} & \frac{2}{\sqrt{3}}V\frac{T}{E} \end{bmatrix} \begin{bmatrix} 1 \\ \cos\theta \\ \sin\theta \end{bmatrix} \tag{1-c}$$

T is the cycle period, V_{ref} is the reference vector, and t_1, t_3 and t_4 are the on-durations of the adjacent switching state vectors V_1, V_3 and V_4, respectively.

It is shown in [5] that for a 2-level inverter, a competitive network can be used to calculate the nonlinear cosine functions from the two winner outputs as follows.

$$\begin{bmatrix} n_i \\ n_{i+1} \end{bmatrix} = \left|\underline{V}_{ref}\right| \cdot \begin{bmatrix} \cos(\theta) \\ \cos(60^\circ - \theta) \end{bmatrix} \tag{2}$$

n_i and n_{i+1} are the winner outputs and are calculated by a very simple and fast algorithm.

To apply the same procedure given in (2), (1-c) must be expressed by $\cos\theta$, and $\cos(60^\circ - \theta)$ instead of $\cos\theta$ and $\sin\theta$. In other words, we can write,

$$\begin{bmatrix} 1 \\ \cos\theta \\ \cos(60^\circ - \theta) \end{bmatrix} = H \begin{bmatrix} 1 \\ \cos\theta \\ \sin\theta \end{bmatrix} \quad where \quad H = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & \frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \tag{3}$$

Combining (1), (2), and (3) results in:

$$\begin{bmatrix} t_1 \\ t_3 \\ t_4 \end{bmatrix} = \begin{bmatrix} T & \frac{4}{3}\frac{T}{E\cdot V} & -\frac{8}{3}\frac{T}{E\cdot V} \\ -T & \frac{4}{3}\frac{T}{E\cdot V} & \frac{4}{3}\frac{T}{E\cdot V} \\ T & -\frac{8}{3}\frac{T}{E\cdot V} & \frac{4}{3}\frac{T}{E\cdot V} \end{bmatrix} \begin{bmatrix} 1 \\ n_i \\ n_{i+1} \end{bmatrix} \tag{4}$$

which is similar to (2), obtained for a two-level SVM implementation.

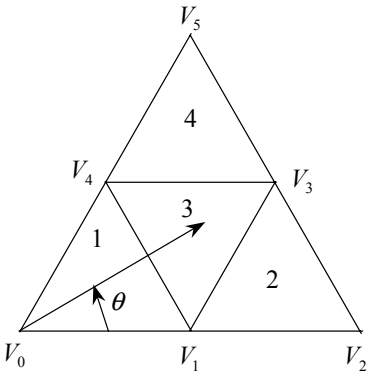


Fig. 3. First switching sector in 3-Level inverters.

C. Distinguishing Between Four distinct Triangles

Fig. 4 shows the proposed structural algorithm to find the triangle number in which the end of the reference vector, V_{ref}, lies. The proposed structure of Fig. 4 consists of four different paths, each one represents one triangular area. When the end of the reference vector lies in one area, corresponding path will have a "1" in its output, while all other paths have "0" in their outputs. Thus, each path is a Classifier Neural Network (CNN) [10], and detects a specified region defined by a triangle. Fig. 5 shows the detailed structure of the third path. The matrix used in this path is a mathematical representation of the neural network used in the proposed structure.

For the third path, this matrix is given in (5):

$$\begin{bmatrix} \sqrt{3} & 1 & -\frac{\sqrt{3}}{2} \\ -\sqrt{3} & 1 & \frac{\sqrt{3}}{2} \\ 0 & -1 & \frac{\sqrt{3}}{4} \end{bmatrix} \quad (5)$$

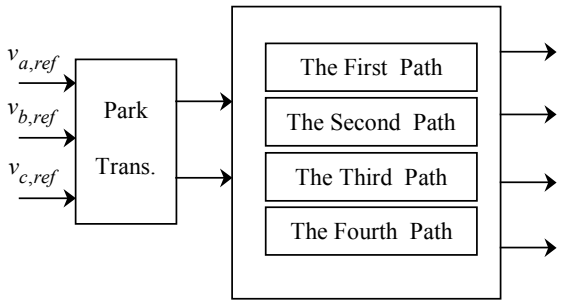


Fig. 4. The proposed four-path structure to detect quadruple triangular regions.

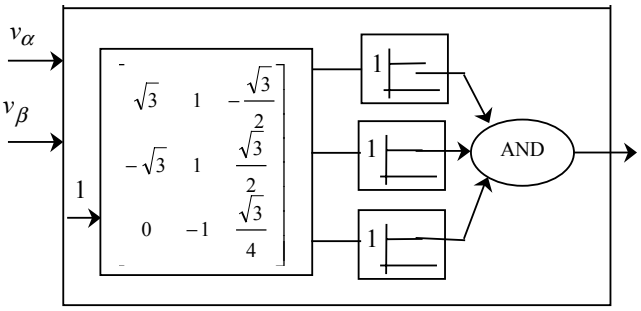


Fig. 5. Detailed third path in the four path structure.

The three remaining paths are designed in the same way, and the coefficients are normalized with respect to the amplitude of the dc bus voltage.

It is worth mentioning that if V_{ref} is placed in another sector, the modified structure of Fig. 6 can be used. This structure has a mapping block. This block maps all other sectors to sector 1 by adding and subtracting appropriate multiples of $\pi/3$ to the phase of V_{ref}.

IV. Proposed SVM Implementation for a M-Level DCMI

A. m-Level Inverter Topology and Switching States

Fig. 7 shows a schematic of one phase of a m-level inverter. Since m different switching states for each phase exist, a three phase m-level inverter has m^3 switching states.

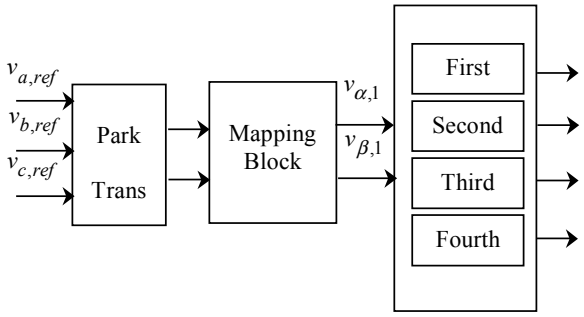


Fig. 6. The modified four path structure to detect quadruple regions.

The application of the Park Transformation to the m^3 permitted switching states of this inverter results in $3m(m\text{-}1)$ non-zero phase voltage space vectors (V_k, k = 1,2,…, $3m(m\text{-}1)$) forming an $(m\text{-}1)$-layer hexagon centered at the origin of $\alpha\beta$ plane and a zero voltage vector located at the origin of the plane. Fig. 8 shows a sector (Sector 1) of this hexagon.

B. Voltage Vectors and Their Durations

Before deriving the on-durations of the different voltage vectors, we describe how to assign a number to each triangle. In m-level inverters, every sector consists of $(m\text{-}1)^2$ triangular areas, and $3m(m\text{-}1)+1$ different voltage vectors. It can be observed, from Fig. 8, that there are $(m\text{-}1)$ layers of triangles, numbered here from 2 to m (q = 2, 3,…, m). Thus, there are $2q\text{-}3$ triangles in the q^{th} layer. These triangles are numbered from 1 to $2q\text{-}3$. With a little attention, one can see that odd numbered triangles have all sides in parallel with the main sides of the sector that passes through origin. While, even numbered triangles have just one side in parallel with a line of the sector which passes the origin. Now, consider the q^{th} layer of this sector. In this layer, the vertices are numbered from P_1 to P_{q-1}. Each vertex identifies triangles, except the $(q\text{-}1)^{th}$ vertex which only identifies one. The on-durations of switching state vectors in each triangle located in the q^{th} layer (q = 2, 3,…, m) with the j^{th} vertex (j = 1, 2,…, q-1) are given by (see Fig. 8):

$$\begin{aligned} &P_j \cdot t_j + P_{j,1} \cdot t_{j,1} + P_{j,2} \cdot t_{j,2} = \underline{V}_{ref} \cdot T \\ &t_j + t_{j,1} + t_{j,2} = T \end{aligned} \quad (6\text{-a})$$

$$\begin{aligned} &\underline{V}_{ref} = V(\cos\theta + i\sin\theta) \\ &V = \left|\underline{V}_{ref}\right| \end{aligned} \quad (6\text{-b})$$

T is the cycle period, $\underline{V}_{ref}$ is the reference vector, and t_j , $t_{j,1}$ and $t_{j,2}$ are the on-durations of P_j , $P_{j,1}$ and $P_{j,2}$ respectively.

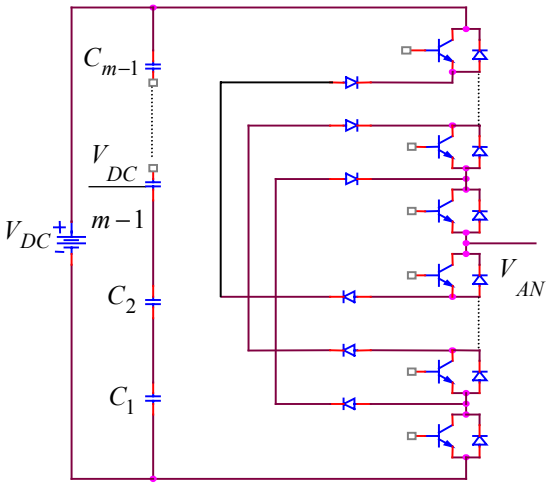


Fig. 7. Schematics of one phase of a m-Level inverter.

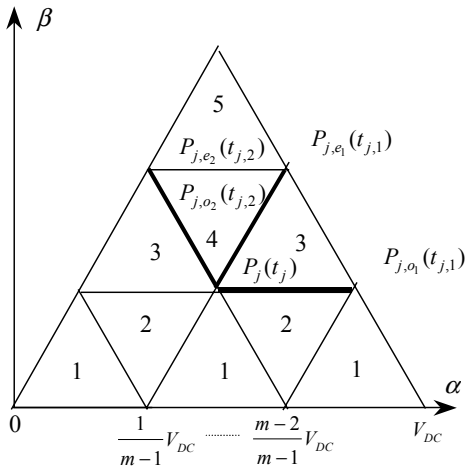


Fig. 8. First sector of a m-Level inverter.

First, consider that the end of the reference vector lies in a triangle with an odd number located in the q^{th} layer with the j^{th} vertex. From (6) we have:

$$\begin{bmatrix} t_j \\ t_{j,1} \\ t_{j,2} \end{bmatrix} = A_1 \cdot \begin{bmatrix} 1 \\ \cos\theta \\ \cos(60^\circ - \theta) \end{bmatrix} \tag{7-a}$$

$$A_1 = \begin{bmatrix} (l-1)T & -\frac{2}{3}\frac{(m-1)VT}{V_{DC}} & -\frac{2}{3}\frac{(m-1)VT}{V_{DC}} \\ (j-l+1)T & \frac{4}{3}\frac{(m-1)VT}{V_{DC}} & -\frac{2}{3}\frac{(m-1)VT}{V_{DC}} \\ (1-j)T & -\frac{2}{3}\frac{(m-1)VT}{V_{DC}} & \frac{4}{3}\frac{(m-1)VT}{V_{DC}} \end{bmatrix} \tag{7-b}$$

Second, consider that the end of the reference vector lies in a triangle with an even number. From (6) we have:

$$\begin{bmatrix} t_j \\ t_{j,1} \\ t_{j,2} \end{bmatrix} = A_2 \cdot \begin{bmatrix} 1 \\ \cos\theta \\ \cos(60^\circ - \theta) \end{bmatrix} \tag{8-a}$$

$$A_2 = \begin{bmatrix} jT & \frac{2}{3}\frac{(m-1)VT}{V_{DC}} & -\frac{4}{3}\frac{(m-1)VT}{V_{DC}} \\ (2-l)T & \frac{2}{3}\frac{(m-1)VT}{V_{DC}} & \frac{2}{3}\frac{(m-1)VT}{V_{DC}} \\ (l-j-1)T & -\frac{4}{3}\frac{(m-1)VT}{V_{DC}} & \frac{2}{3}\frac{(m-1)VT}{V_{DC}} \end{bmatrix} \tag{8-b}$$

The interesting point is that the solution of the $(m\text{-}1)^2$ equations can be obtained with solving just two 3 by 3 equations with two parameters, j and q.

C. Distinguishing Between $(m\text{-}1)^2$ distinct Triangles

As described for a 3-level inverter, a Classifier Neural Network is again used to detect in which triangle the end of the V_{ref} vector lies. A structure similar to that of Fig. 4, but with $(m\text{-}1)^2$ paths is used. Alternatively, a structure with just one path and a recursive algorithm can be used to calculate the outputs of different paths. Then, it is enough to identify the matrices representing side coefficients of each region. Again consider we are at the j^{th} vertex in the q^{th} layer and consider that triangles are numbered consecutively from 1 to $(m\text{-}1)^2$, when moving from the 2^{nd} layer to the m^{th} layer. To represent the side coefficients of the $((q\text{-}2)^2+2(j\text{-}1)+1)^{th}$ and the $((q\text{-}2)^2+2(j\text{-}1)+2)^{th}$ triangles, the distinguishing matrices are given as follows :

$$\begin{bmatrix} 0 & 1 & -\frac{\sqrt{3}}{2}(j-1)\frac{V_{DC}}{m-1} \\ \sqrt{3} & -1 & -\sqrt{3}\frac{V_{DC}}{m-1}(q-j-1) \\ -\sqrt{3} & -1 & \sqrt{3}\frac{q-1}{m-1}V_{DC} \end{bmatrix} \tag{9-a}$$

$$\begin{bmatrix} -\sqrt{3} & 1 & \sqrt{3}(q-j-1)\frac{V_{DC}}{m-1} \\ \sqrt{3} & 1 & -\sqrt{3}\frac{q-2}{m-1}V_{DC} \\ 0 & -1 & \frac{\sqrt{3}}{2}(j)\frac{V_{DC}}{m-1} \end{bmatrix} \tag{9-b}$$

V. Implementation and Simulation Results

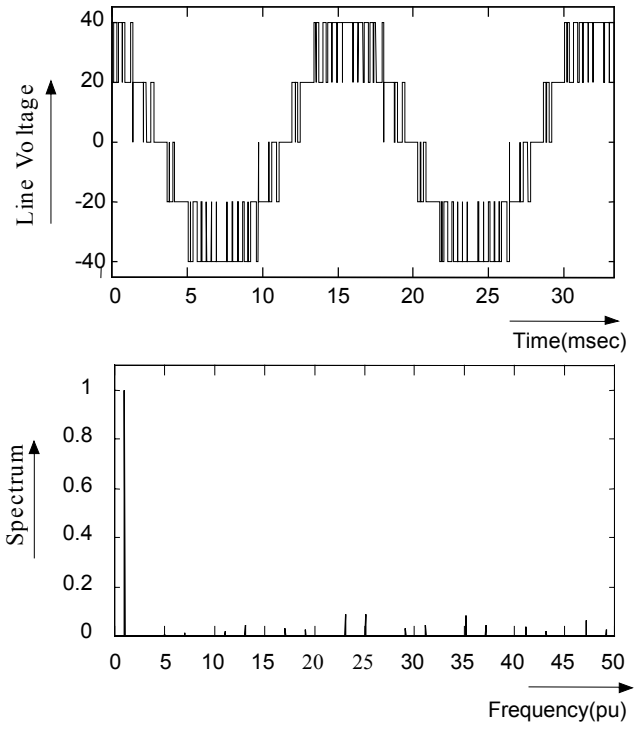
The results obtained from the theoretical and the mathematical analyses are verified by simulations on a 3-level converter structure. Sample simulation results are shown in Fig. 9.

Typical line-line voltages and spectra show that the SVM technique can be appropriately implemented using the proposed classification algorithm on a general *m*-level converter.

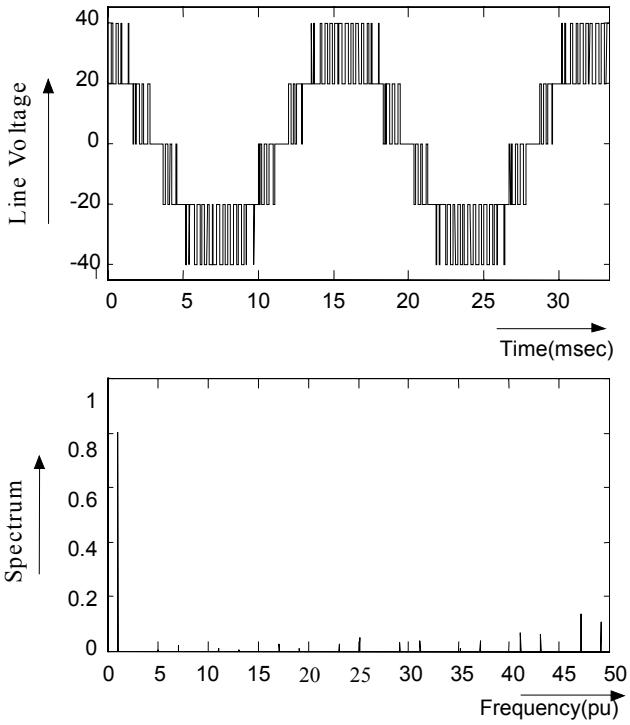
The main differences between the classification and conventional implementation techniques are:

a) The classification algorithm formulated in this paper is universal, and regardless of the *m*, can be used to obtain the switching instants of a general *m*-level converter.

b) In the classification algorithm, non-linear functions and time consuming calculations are avoided. Therefore, this technique reduces hardware and software complexity, decreases the computation time, and increases the accuracy of the positioning of the switching instants.



(a)



(b)

Fig. 9. Simulation results obtained from applying the proposed classification algorithm on a three-level voltage source inverter, line-line voltage and spectra (a) $m_a = 1$ (b) $m_a = 0.8$, f_{sw}=*1440 Hz.*

To compare the proposed SVM with a Sinusoidal Pulse Width Modulated (SPWM) technique, the simulation results obtained on a SPWM modulated 3-level inverter under the same conditions are obtained. Fig. 10 shows the fundamental component of the output voltage as a function of the modulation index obtained for both techniques. Results show that, for the proposed technique:

a) The transfer characteristic is linear.

b) The linear range is wider, resulting in a better utilization of the dc input voltage for high modulation indices (overmodulation).

VI. Conclusion

A universal classification algorithm for the implementation of the space vector modulation on a general multi-level converter is proposed in this paper. The technique employs classifier networks such as are found in neural network theory to distinguish between $6.(m-1)^2$ separate decision areas, in which the tip of the reference voltage vector lies. It generates the switching instants of a general *m*-level converter. The algorithm is formulated in general terms and applies regardless of the number of converter levels *m*.

In addition, non-linear function approximations and time-consuming calculations are avoided. This reduces software complexity, decreases computation time, and increases the accuracy of the positioning of the switching instants. The on-durations of the switching state vectors are calculated by simple mathematical operators such as multiplications and additions.

The algorithm has been implemented on a simulator and the mathematical and theoretical analyses are verified.

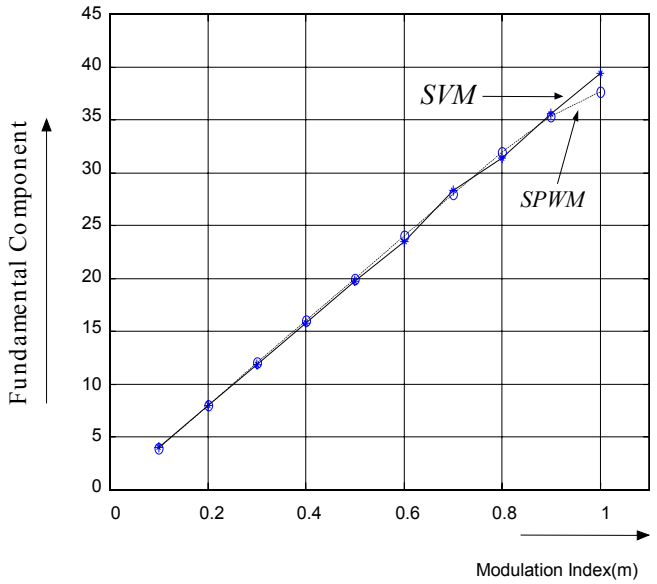


Fig. 10. Comparison between the fundamental components of the output voltage as a function of the modulation index obtained from SVM and SPWM techniques (3-level inverter).

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