A Fast and Universal Neuro-Based SVM Algorithm for Multi-Level Converters

M. Saeedifard, H. Saligheh Rad, A. Bakhshai, and R. Iravani

Abstract— **This paper proposes a novel, simple and fast classification algorithm for implementation of Space Vector Modulation (SVM) method for a Diode Clamped Multi-level Converter (DCMC) with an arbitrary number of levels. The proposed algorithm is based on a classifier neural network which provides a straightforward and computationally efficient approach without the use of trigonometric calculations or look-up tables to identify (i) the location of reference voltage vector, (ii) its adjacent switching voltage vectors, and (iii) their corresponding on-duration time intervals. The feasibility of the proposed SVM algorithm is validated based on theoretical analysis, simulation studies and experimental tests on a DSP-controlled, 5 kVA, three-level converter system.**

Index Terms— Space Vector Modulation, Multi-Level Converters, Competitive Neural Network, Classification Technique.

I. Introduction

THE Diode-Clamped Multi-Level Converter (DCMC) [1] has gained special attention for high power/voltage applications [1]- [5]. In comparison with the conventional two-level topology, the main features of a DCMC are as follows [1], [2]:

- improved AC-side voltage spectrum due to a higher number of converter levels,
- reduced switching dv/dt stresses,
- lower switching devices ratings and lower switching frequency as compared with a two-level converter for the same input-output requirements.

In addition, the DCMC obviates/minimizes the interface transformer. This unique feature reduces the overall system volume and footprint which is of importance for some applications.

Among various multi-level Pulse Width Modulation (PWM) methods [1], [6], Space Vector Modulation (SVM) is the preferred PWM strategy to control the AC-side voltage of a DCMC in view of its flexibility in selecting and optimizing switching patterns for (i) harmonic minimization, and (ii) DC-capacitor voltage balancing [7].

In conventional SVM algorithms, identification of switching voltage vectors that are used to synthesize the reference vector [8] involves identification of sectors and triangles where the tip of the reference vector lies within, and requires look-up table search and multiple trigonometric operations for duty cycle calculation. As the number of converter levels increases, software and hardware complexity for realization of the SVM algorithm significantly increases. Therefore, fast algorithms are required to overcome complexity of calculations and also to fit the entire processing time within a modulation period to leave adequate time for other tasks, e.g. sensing control variables and performing command calculations.

Several SVM algorithms with low computational burden and simplified calculations have been proposed and reported in the technical literature [9]- [17]. In [11] a new coordinate system is constructed to simplify the calculations. However, the duty cycle calculations of the adjacent switching vectors are still relatively complex. In addition, the algorithm needs look-up tables to select adjacent vectors corresponding to the reference vector. Modifications to this SVM algorithm can partially improve computational efficiency [12] and minimize the switching frequency [13]. Another modified SVM algorithm for three-level converters is proposed in [14]. This algorithm is based on decomposition of the SVM hexagon diagram of a three-level converter into that of a two-level converter [15]. Although, the decomposition method can be extended for higher level DCMCs, the computational cost is increased with the number of levels [8].

Several attempts also have been made to use fast Neural Network (NN)-based SVM algorithms. An artificial NN-based SVM for three- and five-level converters is presented in [16] and [17], respectively. This algorithm uses two multi-layer NNs to determine, within each switching period, the switching state voltage vectors adjacent to a reference voltage vector, and calculate their duty cycles. The algorithm has the following drawbacks:

- it requires a training stage for the proposed NN, and
- when the number of levels changes, the SVM algorithm should be accordingly updated, which leads to implementation difficulties in view of its universality.

A fast NN-based SVM algorithm for conventional two-level converters is developed in [18] and [19]. The algorithm uses a classifier NN to identify the switching vectors and calculate their duty cycles. In this paper we propose a classification algorithm that when extended for a general n-level DCMC preserves the features and eliminates drawbacks of the existing SVM algorithms. In addition, it does not exhibit the drawbacks of the NN-based algorithms proposed in [16] and [17]. The proposed classification algorithm for the implementation of SVM strategy for a DCMC is fast, simple to implement,

M. Saeedifard and R. Iravani are with the Center for Applied Power Electronics (CAPE), Department of Electrical and Computer Engineering, University of Toronto, 10 King's College Road, Toronto, Ontario M5S 3G4, Canada (emails: mary.saeedifard@utoronto.ca and iravani@ecf.utoronto.ca).
H. Saligheh Rad is with the Division of Engineering and Applied Sciences, Harvard University, Cambridge, MA 02138, USA (email: hamid@deas.harvard.edu).
A. Bakhshai is with the Department of Electrical and Computer Engineering, Queen's University, Kingston, Ontario, K7L 3N6, Canada (email: alireza.bakhshai@queensu.ca).

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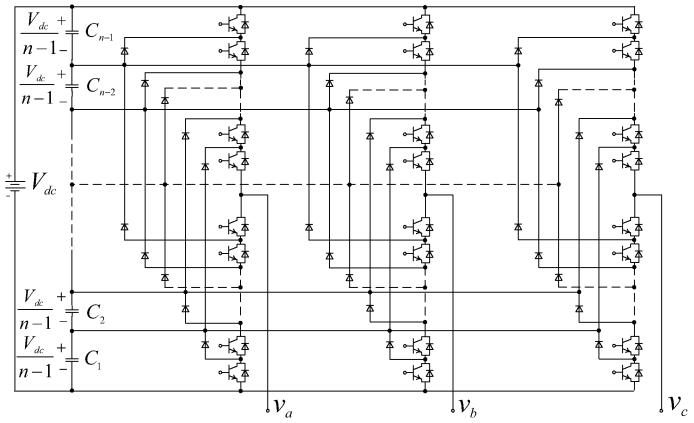


Fig. 1. Schematic representation of a three-phase n-level DCMC

and applicable to three-phase DCMC configurations with any number of levels.

Using the proposed algorithm, the computational overhead of the SVM is performed by a NN through simple mathematical operations. The algorithm avoids trigonometric calculations of SVM and saves considerable processor execution time. Therefore, it permits (i) more sophisticated control techniques and (ii) higher switching frequency. Features of the proposed SVM algorithm is validated by analysis, computer simulations, and experimentation on a 5 kVA three-level converter and reported in this paper.

II. Principles of SVM for a n-level DCMC

A. Space Vector Plane, Sectors, and Switching Voltage Vectors

Fig. 1 shows a schematic diagram of a three-phase n-level DCMC in which the DC-link consists of capacitors $C_1, C_2, ..., C_{n-2}$, and C_{n-1} [12]. Corresponding to the net DC-link voltage of V_{dc}, voltage across each capacitor is ideally $V_{dc}/(n-1)$. Hereinafter, analysis of the n-level DCMC of Fig. 1 is explained with reference to Fig. 2 in which each phase is interfaced to the DC-link terminals through a fictitious n-pole switch. Based on the switching rules of the actual switches of the n-level DCMC of Fig. 1, the switching functions of the n-pole switches of the DCMC of Fig. 2 are defined. Since there are n distinct switching states for each phase of the converter of Fig. 2, the total number of switching state vectors is n^3. Each switching state is represented by (i, j, k) where $i, j, k \in \{0, 1, ..., n-1\}$, and defines positions of the n-pole switches of the three phases.

Applying the Park's transformation to the output phase voltages corresponding to the n^3 switching states results in a set of switching voltage vectors that form a $(n-1)$-layer hexagon centered at the origin of $\alpha\beta$ plane, and n zero voltage vectors located at the origin. The hexagon is divided into six 60° sectors specified by I to VI, Fig. 3.

B. Conventional SVM Algorithm

When the reference voltage vector, V_{ref}, is located in sector I, at any sampling instant the tip of voltage vector lies in a triangle formed by the three switching vectors adjacent to it, Fig. 3. This arrangement which constitute the best set of

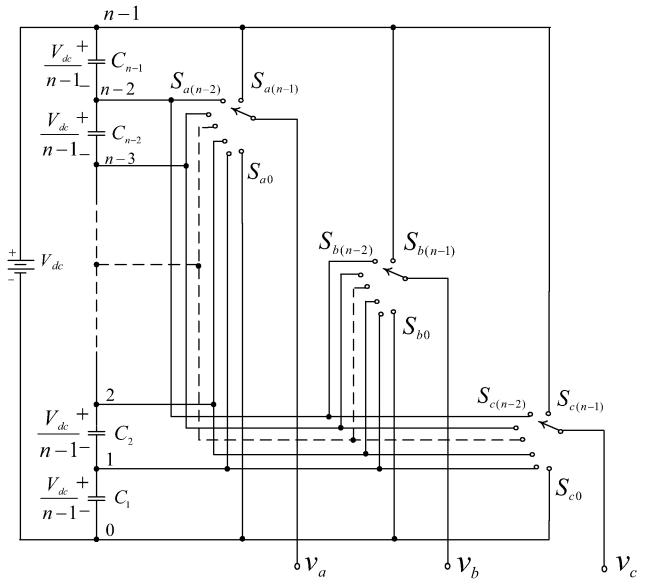


Fig. 2. Schematic representation of the n-level DCMC of Fig. 1 based on n-pole fictitious switches

vectors to synthesize the reference voltage vector [13] based on

$$p_j t_j + p_{j,1} t_{j,1} + p_{j,2} t_{j,2} = V_{ref} \cdot T, \quad t_j + t_{j,1} + t_{j,2} = T, \tag{1a}$$

$$V_{ref} = |V_{ref}| e^{j\theta}, \ \theta = \angle V_{ref}, \tag{1b}$$

$$m = \frac{2}{\sqrt{3}} \frac{|V_{ref}|}{V_{dc}}, \tag{1c}$$

where T is the switching period (cycle period), m is the modulation index, p_j, $p_{j,1}$ and $p_{j,2}$ are the three switching vectors adjacent to the reference voltage vector, and t_j, $t_{j,1}$ and $t_{j,2}$ are the calculated duty cycles of the switching vectors, respectively [13]. The same applies when the tip of the reference voltage is in other sectors.

The computational burden to synthesize a reference voltage is mostly associated with trigonometric calculations for (i) identification of the sector and the triangle in which the tip of the reference vector is located within, (ii) selection of appropriate switching voltage vectors, and (iii) calculation of on-duration time intervals of switching voltage vectors. Moreover, as the triangle in which the tip of the reference vector is located within changes, the equations used for the calculations of on-duration time intervals are changed. Thus, in a conventional SVM, each triangle has its own equations for calculation of the on-duration time intervals. Therefore, as the number of levels of a DCMC increases, the computational burden and the complexity of calculations significantly increase. The following section shows that the aforementioned computational requirement can be substantially reduced by means of a general classification technique.

III. The New SVM Algorithm

References [18] and [19] demonstrate that a SVM algorithm for a conventional two-level converter can be developed by means of a simple classification algorithm based on Kohonen's competitive NN. Kohonen's competitive NN classifies a group

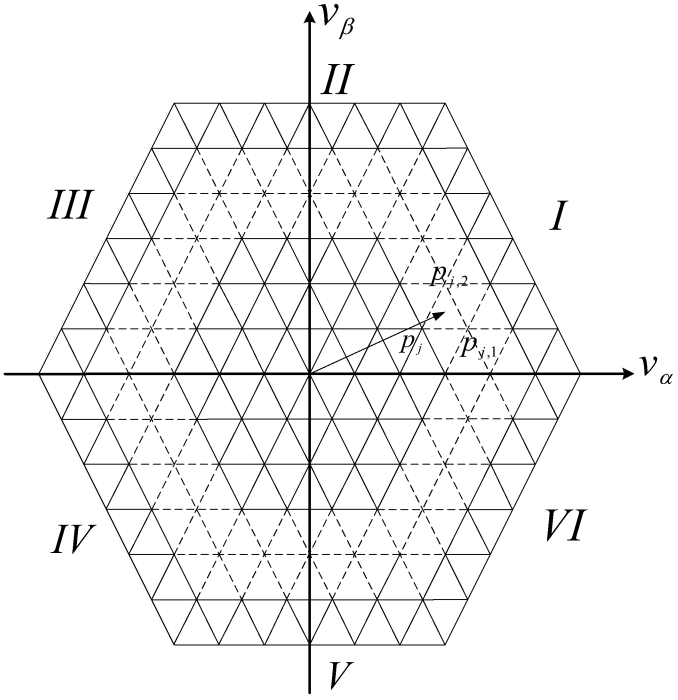


Fig. 3. Representation of space voltage vectors of a n-level DCMC in $\alpha\beta$ plane

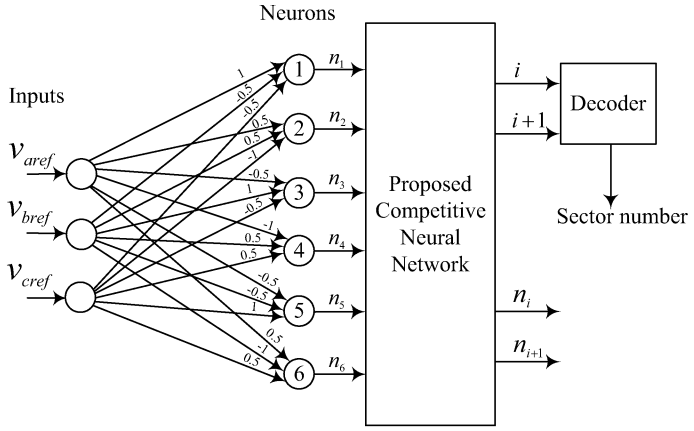


Fig. 4. Schematic diagram of the proposed classification algorithm

of input vectors into a number of class vectors in its training mode, and assigns a class vector to an input vector in its recalling mode. Since a SVM is a deterministic process and all class vectors are known in advance in the Kohonen's competitive NN, there is no need to train the NN. This is a salient feature that is exploited to develop a fast and simple NN-based SVM algorithm. The following section utilizes the advantage of this feature and presents a real-time neuro-computing approach based on a classification algorithm to intelligently identify the desired switching voltage vectors and calculate the corresponding on-duration time intervals.

A. SVM Based on the Kohonen's NN

Fig. 4 shows calculation details of the proposed classification algorithm to efficiently realize a SVM algorithm for a 2-level converter. A reference vector is applied to a NN composed of six computational units, where each unit is associated with a predetermined gain vector. Based on appropriate gain vectors [18], as shown in Fig. 4, the output of the kth unit is the inner product of the reference vector and the kth switching state vector, Fig. 5(a), that is

$$n_k = |V_{ref}||V_k| \cos \angle V_{ref}, V_k), \quad for\ k = 1, 2, ..., 6. \quad (2)$$

In a SVM algorithm for a 2-level converter, out of six class vectors, the two closest vectors to V_{ref} must be specified, therefore, the proposed competitive NN has two winners. Without the loss of generality we can assume that all vectors are normalized and thus inner product (2) can be rewritten as

$$n_k = |V_{ref}| \cos \theta_k). \quad (3)$$

Equation (3) indicate that the closest V_k to V_{ref} generates the largest n_k. The largest n_k and the second largest n_k uniquely specify the two space voltage vectors adjacent to V_{ref}. Therefore, e.g. if reference vector V_{ref} lies in the sector delimited by V_i and V_{i+1}, among all $n_k, k = 1, 2, ..., 6$, n_i and n_{i+1} have the largest positive values. Thus, if the competitive NN selects the two largest n_k's as its two winners, i.e. n_i and n_{i+1}, the two switching vectors which synthesize the output voltage are V_i and V_{i+1}, Fig. 5(b). The corresponding indices of n_i and n_{i+1}, i.e. the class numbers i and $i+1$, specify the sector number in which the tip of V_{ref} is located within.

By the proposed classification technique, the inner product between reference vector V_{ref} and a switching class vector V_k is obtained simply by a linear combination of the three input voltage references, Fig. 4. Outputs of winner units, Fig. 5(b), are given by

$$\begin{bmatrix} n_i \\ n_{i+1} \end{bmatrix} = |V_{ref}| \begin{bmatrix} \cos \theta) \\ \cos(60^\circ - \theta) \end{bmatrix}, \quad (4)$$

From trigonometry, $\cos \theta$ and $\cos(60^\circ - \theta)$ can also be expressed as

$$\begin{bmatrix} \cos \theta) \\ \cos(60^\circ - \theta) \end{bmatrix} = \frac{1}{\sqrt{3}} \begin{bmatrix} 2 & 1 \\ 1 & 2 \end{bmatrix} \begin{bmatrix} \cos(60^\circ - \theta) \\ \sin \theta) \end{bmatrix}. \quad (5)$$

From (5) and (4) we deduce

$$\begin{bmatrix} \cos(60^\circ - \theta) \\ \sin \theta) \end{bmatrix} = \frac{1}{\sqrt{3}|V_{ref}|} \begin{bmatrix} 2 & -1 \\ -1 & 2 \end{bmatrix} \begin{bmatrix} n_i \\ n_{i+1} \end{bmatrix}. \quad (6)$$

In the following section, we show that the proposed classification algorithm can be extended to develop a universal fast SVM algorithm for a n-level DCMC. Equations (4) and (6) will be used to alternatively express the on-duration time intervals of the switching state vectors in terms of the outputs of the competitive neural network, n_i and n_{i+1}.

B. Determination of Reference Vector Location

To identify location of a reference vector, first the sector number is determined based on indices of n_i and n_{i+1}, i.e. i and $i+1$, as shown in Section III-A. Then, the triangle in which the tip of the reference vector is located within, is identified as follows. The reference voltage vector is decomposed into two new vectors along the axes of the θ° coordinates system

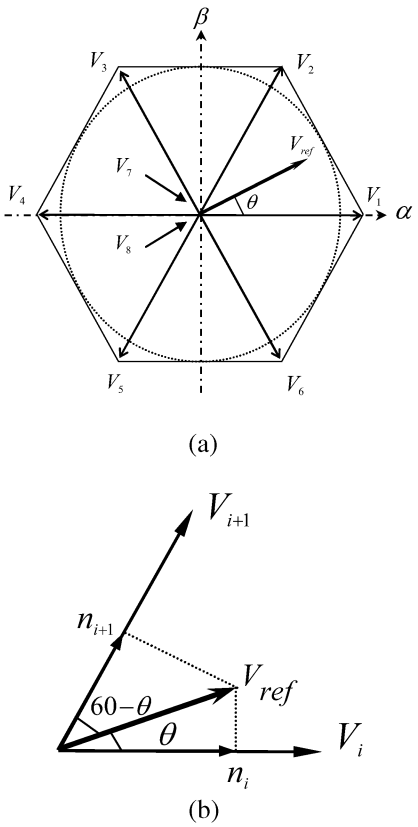


Fig. 5. Representation of reference vector and switching vectors of a 2-level converter in $\alpha\beta$ plane: (a) all sectors, (b) winners of the competition

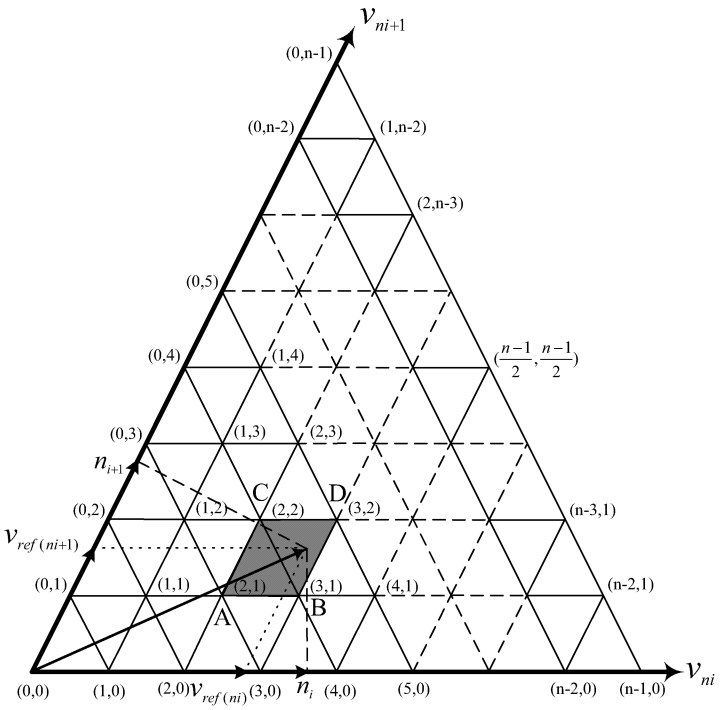


Fig. 6. Space vector representation of an n-level DCMC in the first sector

of sector I, Fig. 6. The lengths of new vectors $V_{ref(ni)}$ and $V_{ref(ni+1)}$ are determined by

$$V_{ref(ni)} = \frac{V_{ref}\cos(60-\theta) - \frac{V_{ref}}{\sqrt{3}}\sin(60-\theta)}{V_d/(n-1)}, \tag{7a}$$

$$V_{ref(ni+1)} = \frac{V_{ref}\cos(\theta) - \frac{V_{ref}}{\sqrt{3}}\sin(\theta)}{V_d/(n-1)}. \tag{7b}$$

By substituting for $\cos(60-\theta), \sin(60-\theta), \cos(\theta)$, and $\sin(\theta)$ from (4) and (6) in (7) we deduce

$$\begin{aligned} V_{ref(ni)} &= \frac{4(n-1)}{3V_d}n_i - \frac{2(n-1)}{3V_d}n_{i+1} \\ &= \frac{2(n-1)}{3V_d}(2n_i - n_{i+1}), \end{aligned} \tag{8a}$$

$$\begin{aligned} V_{ref(ni+1)} &= -\frac{2(n-1)}{3V_d}n_i + \frac{4(n-1)}{3V_d}n_{i+1} \\ &= \frac{2(n-1)}{3V_d}(-n_i + 2n_{i+1}). \end{aligned} \tag{8b}$$

Fig. 6 shows winners of the competitive NN of Fig. 4, n_i and n_{i+1}, reference voltage vector V_{ref}, and its decomposed components $V_{ref(ni)}$ and $V_{ref(ni+1)}$ in terms of n_i and n_{i+1}, obtained from projection (8). Interestingly, based on (8), all sectors are mapped into sector I and consequently the number of triangular regions are substantially reduced. Moreover, the reference vector is located in a diagram in which the triangular regions have unity length and the coordinates of voltage vectors are integer values. At any instant, the tip of reference vector is located in a parallelogram formed by four voltage vectors, e.g. vertices A, B, C, and D in Fig. 6. Based on (8), calculation of $V_{ref(ni)}$ and $V_{ref(ni+1)}$ in terms of n_i and n_{i+1} determines vertices of the parallelogram. Let's define

$$l_1 = int(V_{ref(ni)}), \tag{9}$$

$$l_2 = int(V_{ref(ni+1)}), \tag{10}$$

where $int()$ is a lower rounded integer function. Thus, coordinates of vertices A, B, C, and D are calculated as

$$(V_{A(ni)}, V_{A(ni+1)}) = (l_1, l_2), \tag{11a}$$

$$(V_{B(ni)}, V_{B(ni+1)}) = (l_1, l_2+1), \tag{11b}$$

$$(V_{C(ni)}, V_{C(ni+1)}) = (l_1+1, l_2), \tag{11c}$$

$$(V_{D(ni)}, V_{D(ni+1)}) = (l_1+1, l_2+1). \tag{11d}$$

To determine if the reference vector is located in the triangle formed by either A, B, and C or B, C, and D vertices, the logic is:

$$\begin{aligned} &V_{ref} \text{ is in ABC triangle if :} \\ &\quad V_{ref(ni)} + V_{ref(ni+1)} \geqslant l_1 + l_2 + 1 \end{aligned} \tag{12}$$

$$\begin{aligned} &V_{ref} \text{ is in BCD triangle if :} \\ &\quad V_{ref(ni)} + V_{ref(ni+1)} < l_1 + l_2 + 1 \end{aligned} \tag{13}$$

The process outlined in the section completes identification of the location of the reference voltage vector of a n-level DCMC.

C. Duty-Cycle Calculations

On-duration time intervals of the switching voltage vectors adjacent to the reference voltage vector V_{ref} for a n-level DCMC are calculated as follows. If the tip of the reference voltage vector lies in the ABC triangle, Fig. 6, according to

(1) we have

$$V_A t_A + V_B t_B + V_C t_C = V_{ref} T, \quad t_A + t_B + t_C = T, \tag{14}$$

where t_A, t_B, and t_C are the on-duration time intervals of switching vectors V_A, V_B, and V_C, respectively. Expanding (14) based on v_{ni}- and v_{ni+} -axis components in the 60° coordinates system, Fig. 6, we deduce

$$\begin{aligned} &V_{A(ni)} t_A + V_{B(ni)} t_B + V_{C(ni)} t_C = V_{ref(ni)} T, \\ &V_{A(ni+)} t_A + V_{B(ni+)} t_B + V_{C(ni+)} t_C = V_{ref(ni+)} T, \\ &t_A + t_B + t_C = T. \end{aligned} \tag{15}$$

Substituting for v_{ni}- and v_{ni+} -axis components of V_A, V_B, and V_C from (11) into (15), the on-duration time intervals are

$$\begin{aligned} t_B &= (V_{ref(ni)} - V_{A(ni)})T, \\ t_C &= (V_{ref(ni+)} - V_{A(ni+)})T, \\ t_A &= T - (t_B + t_C). \end{aligned} \tag{16}$$

Similarly, if the tip of the reference voltage vector lies in the BCD triangle, the on-duration time intervals of switching vectors V_B, V_D, and V_C are

$$\begin{aligned} t_B &= (V_{A(ni+)} + V_{ref(ni+)})T, \\ t_C &= (V_{A(ni)} + V_{ref(ni)})T, \\ t_D &= T - (t_B + t_C). \end{aligned} \tag{17}$$

The salient feature of the proposed algorithm is its inherent simplicity. Unlike the conventional SVM algorithms that require solution of several sets of trigonometric equations for calculation of on-duration time intervals, (16) and (17) only depend on two sets of equations to determine the on-duration time intervals. Therefore, the proposed SVM algorithm is much simpler and easier for digital implementation since it reduces the hardware and software complexity and decreases the required computational time.

D. Mapping Adjacent Vectors to Switching States

The last step of the proposed algorithm is to identify switching combinations that correspond to the already determined three adjacent voltage vectors, Section III-B. Since coordinates of the adjacent switching vectors in the 60° coordinates system of Fig. 6 are known, the available switching combinations for a given space vector (v_{ni}, v_{ni+}) are determined by

$$[v_a, v_b, v_c] = [k, k - v_{ni}, k - v_{ni} - v_{ni+}], \tag{18}$$

where $k, k - v_{ni}, k - v_{ni} - v_{ni+} \in [0, 1, ..., n-1]$.

As discussed in Section III-B, the proposed algorithm inherently maps all sectors to the 60° coordinates system of sector I. Since at any instant the number of sector in which the reference vector is located within is identified by the output of the NN block of Fig. 4, and the corresponding switching combinations in other sectors are determined simply by interchanging the switching combinations resulted based on (18). Table I provides the corresponding switching combinations of the converter in all sectors.

Unlike other fast NN-based algorithms [16], [17], sector identification is an inherent feature of the proposed classification technique. This salient feature is particularly advantageous for voltage balancing of DC-capacitors [13].

TABLE I: RELATIONSHIP BETWEEN SWITCHING STATES IN VARIOUS SECTORS

Sector	Phase A	Phase B	Phase C
I	v_a	v_b	v_c
II	$-v_b + n - 1$	$-v_c + n - 1$	$-v_a + n - 1$
III	v_c	v_a	v_b
IV	$-v_a + n - 1$	$-v_b + n - 1$	$-v_c + n - 1$
V	v_b	v_c	v_a
VI	$-v_c + n - 1$	$-v_a + n - 1$	$-v_b + n - 1$

IV. Simulation and Experimental Results

To verify the feasibility and validity of the proposed SVM algorithm, a set of simulation studies and the corresponding experimental case studies were conducted. Comparison of the experimental and simulation results is presented here. Experimental results were obtained from the implementation of the proposed classification algorithm on a 5 kVA, three-level converter setup. A control platform based on TMS320C31 DSP (60 MHz clock frequency) was employed to implement the control algorithms and to test performance of the proposed SVM algorithm.

The simulation results of the three-level converter for modulation index of $m = 0.8$, and switching frequency of $f_{sw} = 2.8$ kHz, is presented in Fig. 7(a). Fig. 7(a) depicts normalized AC-side voltage and its spectrum. To show that the proposed algorithm is general and applicable to the DCMCs with any number of levels, simulation results for four- and five-level DCMCs, and for the same modulation index at switching frequency of $f_{sw} = 2.8$ kHz, are presented in Figs. 7(b) and (c). The multi-level voltage waveforms of Fig. 7 agree with analytical waveforms and show feasibility of the proposed algorithm for DCMCs with different number of levels.

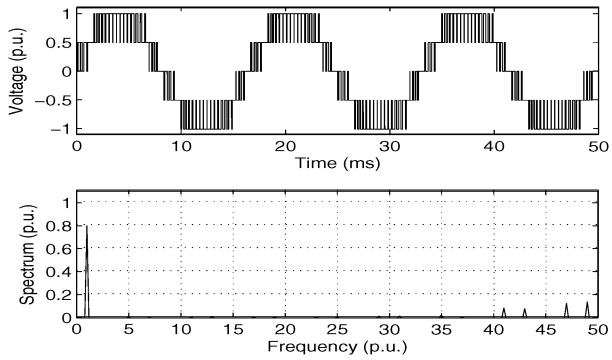
The results of the experimentally measured normalized AC-side voltages and their spectra for different values of modulation indices are shown in Figs. 8 to 10. The corresponding experimental waveforms of Figs. 8 to 10 demonstrate feasibility of the proposed classification algorithm for real-time implementation.

To demonstrate superiority of the classification algorithm over the conventional algorithm in terms of computational time requirements for real-time implementation, the conventional SVM algorithm was also implemented on the DSP control platform. The required DSP software for the proposed SVM algorithm includes 106 instructions, while that of the conventional SVM includes more than 250 instructions. Although the software of the proposed algorithm is not a fully optimized one, the number of its instructions is significantly less than that of the conventional algorithm.

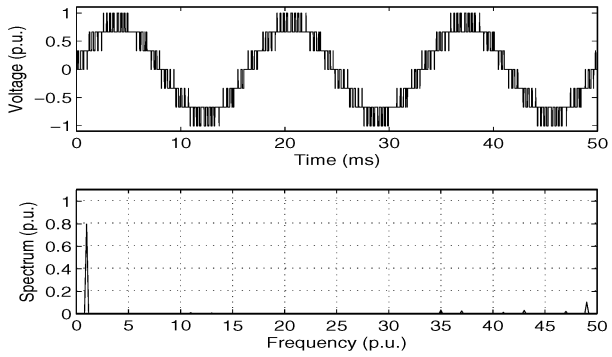
Fig. 11 depicts phase-a gating signals of the three-level converter switches. Although superiority of the proposed SVM algorithm cannot be demonstrated by a single number, the timing diagram of Fig. 12 shows that when compared with the conventional SVM algorithm, the proposed algorithm improves the calculation overhead time and consequently the maximum attainable switching frequency can be increased.

V. Conclusions

In this paper, a general, simple and fast NN-based SVM algorithm for implementation of Space Vector Modulation



(a)



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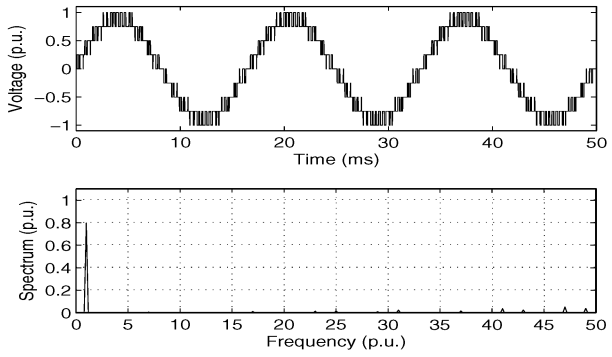
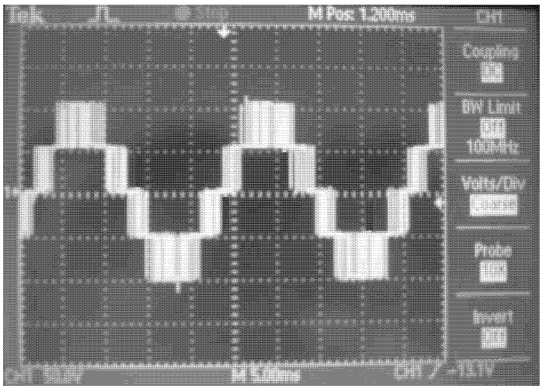


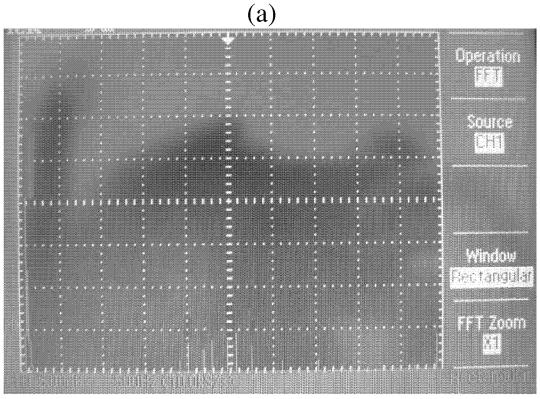
(c)

Fig. 7. **Simulation results:**AC-side voltages and their spectra of (a) 3-level, (b) 4-level, and (c) 5-level DCMCs; m = .8, f_{sw} = Hz

(SVM) algorithm for a n-level Diode Clamped Multi-level Converter (DCMC) is presented. The algorithm uses a simple classifier Neural Network (NN) to identify the switching vectors and calculate their on-duration time intervals. This paper demonstrates that the classification algorithm preserves merits and eliminates the drawbacks of the existing SVM algorithms. In particular, sector identification is an inherent feature of the classification technique. This feature is advantageous for DC-side capacitor voltage balancing, and also for other applications such as 60 degree voltage clamping. To the best of our knowledge, other NN-based fast algorithms do not offer these features. In addition, the proposed technique neither needs a training stage nor requires a change in the algorithm as the number of levels of the DCMC changes

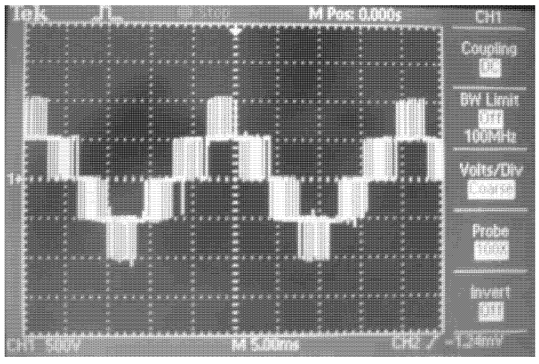


(a)

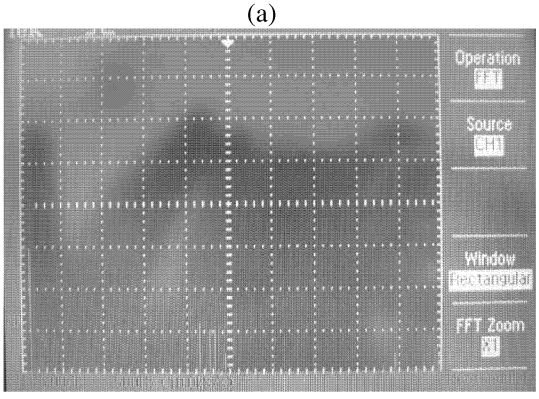


(b)

Fig. 8. **Experimental results:** AC-side voltage of a 3-level DCMC and its spectrum; m = .8, f_{sw} = Hz

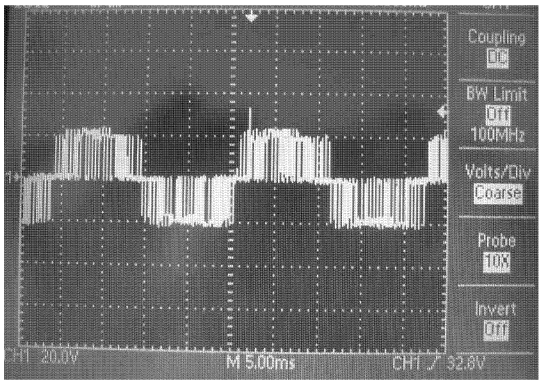


(a)

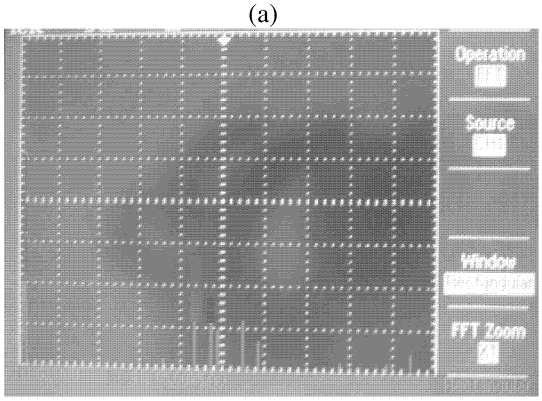


(b)

Fig. 9. **Experimental results:** AC-side voltage of a 3-level DCMC and its spectrum; m = .6, f_{sw} = Hz



(a)



(b)

Fig. 10. **Experimental results:** AC-side voltage of a 3-level DCMC and its spectrum; m = .4, f_{sw} = Hz

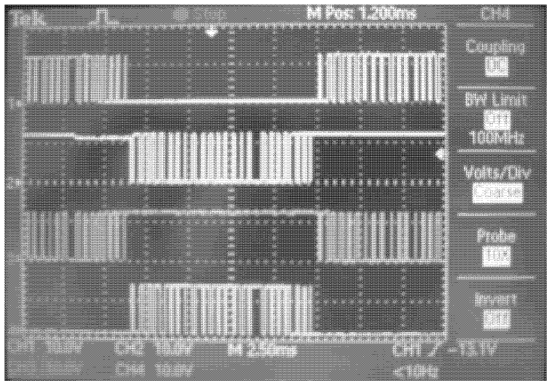


Fig. 11. **Experimental results:** Gating signals of one leg of a 3-level DCMC; m = .8, f_{sw} =

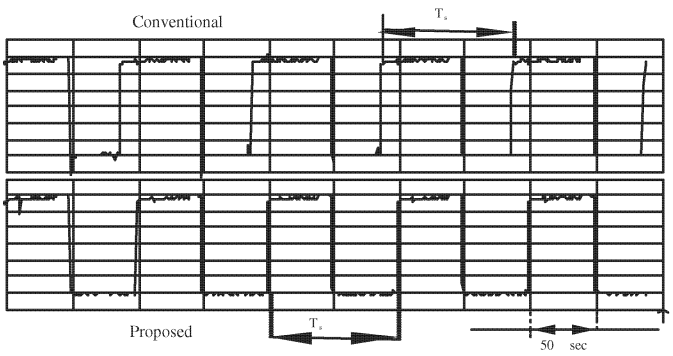


Fig. 12. **Experimental results:** Comparing the minimum possible sampling time between the two SVM algorithms

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